**EXPEDITED PROCEDURE – EXAMINING GROUP 1722**

**S/N 10/750,534** **PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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| Applicant: | Peter A. Davison et al. | Examiner: | Maria Veronica Ewald |
| Serial No.: | 10/750,534 | Group Art Unit: | 1722 |
| Filed: | December 31, 2003 | Docket No.: | P17166 |
| Title: | COMPONENT PACKAGING APPARATUS, SYSTEMS, AND METHODS | | |
| Customer Number: 59796 | | | |

**AMENDMENT & RESPONSE UNDER 37 C.F.R. 1.116**

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In response to the Final Office Action mailed March 26, 2008, please amend the application as follows:

## IN THE DETAILED DESCRIPTION

Please amended the Detailed Desctipton as follows:

Please amend paragraph [0027] as follows:

[0027] The terms substrate or core generally refer to the physical structure or layer that is the basic workpiece that is transformed by various process operations into the desired microelectronic configuration. Substrates may include conducting material (such as copper or aluminum), insulating material (such as sapphire, ceramic, or plastic), semiconducting materials (such as silicon), non-semiconducting materials, or combinations of semiconducting and non-semiconducting materials. In some embodiments, substrates include layered structures, such as a core sheet or piece of material (such as iron-nickel alloy) chosen for its a coefficient of thermal expansion (CTE) that more closely matches the CTE of an adjacent structure such as a silicon processor chip. In some embodiments, such a substrate core is laminated to a sheet of material chosen for electrical and/or thermal conductivity (such as a copper or aluminum alloy), which in turn is covered with a layer of plastic chosen for electrical insulation, stability, and embossing characteristics. In some embodiments, the plastic layer has wiring traces that carry signals and electrical power horizontally (i.e., parallel to the first major surface), and vias that carry signals and electrical power vertically (i.e., perpendicular to the first major surface) between layers of traces.

Please amend paragraph [0028] as follows:

[0028] The term vertical is defined to mean substantially perpendicular to the first major surface of a substrate, while the term horizontal is defined to mean substantially parallel to the first major surface of a substrate. Height or depth refers to a distance in a direction perpendicular to the first major surface of a substrate.

Please amend paragraph [0052] as follows:

[0052] In some embodiments, substrate 1000 is used as starting substrate base 301 for a subsequent deposition of one or more further layers of dielectric and conductive traces/wires on one or both of the first and second major surfaces of the substrate.

Please amend paragraph [0069] as follows:

[0069] Some embodiments provide an apparatus including an embossing tool substrate made of a first metal, [[a]] first and second major surfaces ~~surface~~ of the substrate having an embossing profile, a first coating on the first and second major surfaces ~~surface~~ of the substrate, the first coating providing an adherable surface, and a second coating on the first coating, the second coating providing a non-adhesive outer surface. In some such embodiments, the second coating includes poly-para-xylylene. In some such embodiments, the second coating includes Parylene Nova HT.

Please amend paragraph [0073] as follows:

[0073] Some embodiments provide a method that includes providing an embossed tool substrate 110, depositing a first coating 220 over the first and second major surfaces ~~surface~~ of the substrate, the first coating providing an adherable surface, and depositing a second coating 230 over the first coating 220, the second coating 230 providing a non-adhesive outer surface 231.